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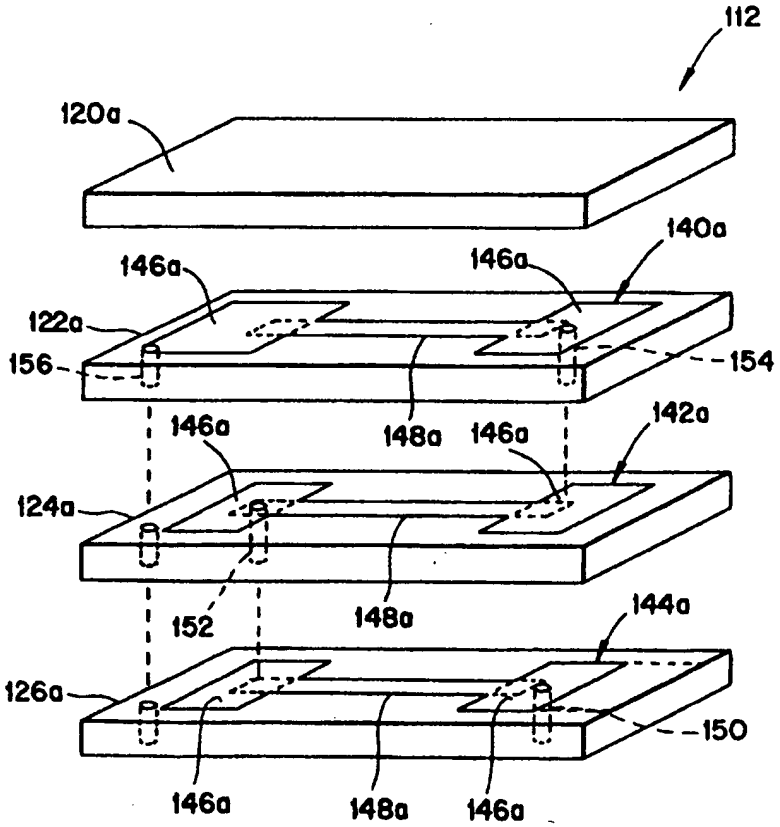
(57) Abstract

A subminiature circuit protector (10) includes at least one layer of ceramic material having at least one fuse element (24) and a cover (20) in a laminate structure. The ends (12, 14) of laminate structure are coated with electrically conductive end terminations (30, 32). Where a layer has more than one fuse element (24), the fuse elements may be connected in parallel or interconnected in series. Each of the fuse elements (24) of the individual layers may comprise two or more individual fuse elements connected in series or parallel. A method for manufacturing the circuit protector (10) includes the steps of printing a multiplicity of fuse elements (24) on a plurality of green ceramic substrates (40), stacking the substrates (40) to form a laminate structure (60), cutting the laminate (60) into individual units (70), firing the individual units (70), and coating the opposite ends (12, 14) of the units with electrically conductive material to form end terminations (30, 32).



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IMPROVEMENTS IN CERAMIC CHIP FUSES

FIELD OF THE INVENTION

The present invention relates to a circuit protector. More particularly, the present invention relates to ceramic chip circuit protectors having current carrying elements on one or more substrate layers. The invention also relates to methods for manufacturing ceramic chip circuit protectors in accordance with the present invention.

BACKGROUND OF THE INVENTION

Subminiature circuit protectors are useful in applications in which size and space limitations are important, for example, on circuit boards for electronic equipment, for denser packing and miniaturization of electronic circuits. Subminiature circuit protectors, or chip fuses, have a smaller footprint than other types of fuses and generally require less horizontal space or "real estate" on the circuit board than conventional fuses.

As voltage and current requirements for a fuse increase, typically a fuse of greater size, in length and diameter, must be provided to meet the needed capacity. In such cases, size and space problems in

circuit boards and other similar applications may be exacerbated.

Ceramic chip type fuses are typically manufactured by depositing layers of metal elements on a ceramic or glass substrate plate, attaching an insulating cover over the deposited layers, and cutting, or dicing, individual fuses from the finished structure. The cutting operation is difficult and expensive to carry out. In addition, subminiature fuses made with deposited film fuse elements are generally limited to low voltage and current interrupting capacity.

SUMMARY OF THE INVENTION

The present invention, generally, provides a method of manufacturing a subminiature surface mountable circuit protector that is simple and relatively inexpensive. The present invention also provides a subminiature circuit protector that has improved short circuit current interrupting capacity compared to conventional circuit protectors of similar physical size.

More particularly, the present invention provides a method of manufacturing a multiplicity of subminiature circuit protectors from a plate of

substrate material that facilitates the formation and rapid cutting of the substrate into individual units.

The present invention also provides a subminiature surface mountable circuit protector for high voltage and/or high current use that is compact and small in size. A subminiature surface mountable fuse in accordance with the present invention comprises a fuse element disposed on a substrate and connected to contact pads at opposite ends of the substrate. Alternatively, the fuse may comprise a plurality of layers of ceramic substrate, with a fusible element disposed on surfaces of at least some of the layers. The fusible elements of different layers may be interconnected in series or in parallel depending on a desired voltage and/or current carrying capacity of the fuse.

According to one aspect, at least some layers of a fuse have a single fuse element thereon. Alternatively, fusible elements are provided on at least some layers of a fuse and comprise two or more fusible elements interconnected in series. A plurality of layers of series connected fusible elements may be connected in parallel to form a single chip fuse.

In another aspect of the invention, the fusible elements may comprise two or more fusible elements

connected in parallel. A plurality of layers of connected fusible elements may be connected in series in a single chip fuse.

According to a method of the present invention, a substrate plate of green, or unfired, ceramic material is prepared. Electrically conductive metallic film is deposited on a top surface of the substrate plate in equally spaced, parallel columns. Fuse elements, in the form of electrically conductive wires or printed elements, are disposed on the top surface of the substrate perpendicular to the film columns, in equally spaced parallel rows. A second plate of green ceramic material is laminated to the substrate over the film columns and fuse elements rows. The second plate covers and encapsulates the film columns and fuse rows.

The thus formed structure is then die cut, that is, cut, longitudinally through the metal film columns and transversely between the fuse element rows so that individual units are produced having strips of metal film at opposite ends and a fuse element extending from end to end across a space between the metal film strips. The die cut individual units are fired to cure the ceramic substrate and cover plate and to cause an intermetallic bond to form between the fuse elements

and the metal film. The ends of the individual units are coated with electrically conductive materials to form electrical terminations for connecting in a circuit.

According to one aspect of the invention, wire fuse elements may be applied to the substrate by rolling and pressing a wire into the substrate. The application of pressure imbeds the wire elements in the substrate and helps form contact between the wire elements and the metallic film.

According to another aspect of the invention, the laminate structure is die cut so that the individual units formed have opposite ends faces and opposite lateral faces. A metal strip at each opposite end of each unit extends to the end face and to both lateral faces so that the electrical termination coatings applied to the units contact the metal strips on the end and lateral faces.

According to yet another aspect of the invention, the end termination coatings comprise a first coating of silver or a silver alloy. A second coating of nickel is applied over the first coating. A third coating of a tin/lead alloy is applied over the nickel coating.

According to a method for preparing multiple layer fuses, a substrate plate of green, or unfired,

ceramic material is prepared. Electrically conductive metallic film is deposited on a top surface of the substrate plate in equally spaced, preferably parallel columns. Fuse elements, in the form of a electrically conductive film, are disposed on the top surface of the substrate in a direction substantially transverse, and preferably perpendicular to a direction of the film columns, in equally spaced, preferably parallel rows. A plurality of substrates thus prepared are positioned in a stack with the columns and rows aligned to form a laminate structure. A cover of green ceramic material is laminated to a top substrate. The formed structure is then cut by a suitable method, preferably longitudinally through the metal film columns and preferably transversely between the fuse element rows so that individual chip fuse units are produced having strips of metal film at opposite ends and a fuse element extending from end to end across a space between the metal film strips. The individual units are fired to cure the ceramic substrate layers and cover and to cause a metallic bond to form between the fuse elements and the metal film. The ends of the individual units are ordinarily coated with electrically conductive materials to form

electrical terminations for connecting the fuse elements.

According to another aspect of the invention, the individual chip fuse units have opposite ends faces and opposite lateral faces. The laminate structure is cut so that a metal strip at each opposite end of each unit extends to the end face and to both lateral faces so that the electrical termination coatings that are ordinarily applied to the units contact the metal strips on the end and lateral faces. This configuration connects the fuse elements to form a parallel configuration.

According to another aspect of the invention, holes are formed by a suitable method, such as by punching, or by being formed with a laser or water jet, in the green ceramic substrate at predetermined locations. The holes are metallized, that is, electrically conductive metal is disposed in the holes by a vacuum drawing method or other suitable technique. Electrically conductive film is deposited on the surface of a substrate in a column of separate pads, so that pads contact predetermined metallized holes. Fuse element material is deposited to connect two pads. Alternatively, the fuse element material is deposited first, and the film is deposited afterwards, or the fuse element material and film are

deposited together. A laminate structure is made of a plurality of substrates overlaid so that pads and fuse elements of stacked layers are in alignment.

The laminate structure is cut so that a pattern of pads, fuse elements and metallized holes form an electrical pathway. The cut individual units are fired to cure the ceramic substrate and cover plate and to cause a metallic bond to form between the metallized holes, fuse elements and the metal film at areas of mutual contact. The ends of the individual units are ordinarily coated with electrically conductive materials to form electrical terminations for completing a series circuit in each fuse.

BRIEF DESCRIPTION OF THE DRAWING FIGURES

The present invention can be further understood with reference to the following description in conjunction with the appended drawings, wherein like elements are provided with the same reference numerals. In the drawings:

Fig. 1 is a perspective view of a circuit protector manufactured according to the present invention;

Fig. 2 is a sectional view of the circuit protector of Fig. 1 taken along line 2-2;

Fig. 3 is a sectional view of the circuit protector taken along line 3-3 of Fig. 2;

Fig. 4 is a top view of a substrate plate illustrating a depositing step of the present invention;

Fig. 5 is a top view of the substrate plate of Fig. 4 after a subsequent step;

Fig. 6 is an end view of a laminate structure of the substrate plate of Figs. 4 and 5 and a cover plate;

Fig. 7 is an end view of the laminate structure of Fig. 6 perpendicular to the view of Fig. 6; and

Fig. 8 is a perspective view of an individual fuse unit produced from the laminate structure of Figs. 6 and 7.

Fig. 9 is a perspective view of a multiple layer circuit protector according to the present invention;

Fig. 10a is a sectional view of the circuit protector of Fig. 9 taken along line 10-10 illustrating a first embodiment of the circuit protector in accordance with the invention;

Fig. 10b is a sectional view of corresponding to the view of Fig. 10a, illustrating an alternative embodiment of a circuit protector according to the invention;

Fig. 11 is an exploded view of a circuit protector according to the invention;

Fig. 12 is a top view of a substrate layer having two fuse elements in series;

Fig. 13 is a top view of a substrate layer having two fuse elements in parallel;

Fig. 14 is a top view of a substrate plate illustrating a depositing method for the circuit protector of Fig. 10a; and

Fig. 15 is a top view of a substrate plate of illustrating a depositing method for the circuit protector of Fig. 10b; and

Fig. 16 is a sectional view of a multiple layer circuit protector according to an embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Fig. 1 is a perspective view of a subminiature circuit protector 10, or fuse, manufactured according to the method of the present invention. The chip fuse 10 is not shown to scale, and the size and thickness of various components of the fuse 10, and the other embodiments further described and illustrated below, are exaggerated for clarity of the illustration.

The fuse 10 of Fig. 1 illustrates a first embodiment having one fuse element disposed on one substrate layer. The fuse 10 includes an upper plate 20 and a lower plate 22 laminated together. End terminations 30, 32, at opposite ends of the fuse 10 electrically connect with the interior components of the fuse 10, not illustrated in this figure. The end terminations 30, 32 also allow the fuse 10 to be connected in an electric circuit.

Fig. 2 is a sectional view of the fuse 10 of Fig. 1 taken along the line 2-2 of Fig. 1. Fig. 3 is a sectional view taken along the line 3-3 of Fig. 2. Between the upper plate 20 and the lower plate 22 of the fuse 10 is disposed a fuse element 24 that extends from one end face 12 to an opposite end face 14 of the fuse. The fuse element 24 in the illustrated embodiment is in the form of a wire. Strips of metal film 26, 28 are disposed at end portions of the fuse 10 in contact with opposite ends of the wire fuse element 24. The metal strips 26, 28 each extend to one end face 12 (or 14) of the fuse 10 and to both lateral faces 16, 18. The metal strips 26, 28 contact the end terminations 30, 32 at the end faces 12, 14 and the lateral faces 16, 18 to form an electrical connection through the fuse 10.

The end terminations 30, 32 are formed of three layers of electrically conductive material. A first, or inner layer 34, comprises a coating of silver or a silver alloy. A second layer 36 comprises nickel and a third layer 38 comprises a layer of tin/lead alloy that facilitates connecting the fuse 10 in an electrical circuit by soldering or other suitable means.

The wire fuse element 24 may be selected to have a desired diameter to provide a predetermined response to current and voltage. Alternatively, the fuse element may be a deposited film or other suitable material having predetermined characteristics.

Figs. 4-7 illustrate a method of manufacturing the fuse 10 of the present invention. The method permits the manufacture of a multiplicity of individual fuses starting with a single substrate plate. Fig. 4 is a top view of a substrate ceramic plate 40 illustrating initial steps of the method. According to the present invention, a substrate plate 40 of green, or unfired, ceramic material having an upper surface 42 is first prepared. Electrically conductive metal film is deposited on the upper surface 42 as a plurality of parallel, spaced columns

44. The metal film columns 44 may be applied by screen printing or another suitable method.

Fig. 5 is a top view of the substrate plate 40 of Fig. 4 illustrating a subsequent step of the method. After the metal film columns 44 are deposited on the upper surface 42, a plurality of wire elements 50 are disposed on the upper surface 42 perpendicular to the metal film columns 44, and in mutually spaced relationship. The wire elements 50 extend across and contact the metal film columns 44. In a preferred embodiment of the method, the wire elements 50 are applied with a rolling applicator which moves across the substrate plate 40 and imbeds the wire element in the substrate as it travels. The wire elements 50 may also be applied by another suitable method.

The wire elements 50 may also be pressed into the upper surface 42 of the substrate plate 40. Green ceramic material is relatively soft and pliable, and pressing the wire elements 50 imbeds the wire elements 50 in the substrate plate 40 to help secure it in place. Pressing the wire elements 50 also helps to make good contact between the wire elements 50 and the metal film 44.

After the metal film columns 44 and the wire element rows 50 are in place on the upper surface 40

of the substrate, a second plate 48 of green ceramic material is laminated on the upper surface 42 of the lower plate 40, as shown in Fig. 6 and Fig. 7. Figs. 6 and 7 are end views of the laminate structure 60. The second plate 48 covers and encapsulates the wire elements 50 and the metal film columns 44. As shown in Figs. 6 and 7, the wire elements 50 and the metal film columns 44 extend to end faces of the laminate structure.

The laminate structure 60 is then die cut to produce individual fuse units. Fig. 8 illustrates an individual unit 70 cut from the laminate structure 60. A steel rule die, or other suitable tool, is used to cut the laminate structure 60 along the broken lines illustrated in Figs. 6 and 7. Each individual unit 70 produced has strips 26, 28 of the metal film at opposite end portions and a wire element 24 extending from one end face 12 to an opposite end face 14. As illustrated, the metal strips 26, 28 also extend to the end faces 12, 14 and to the opposite lateral faces 16, 18 of the unit.

Die cutting the laminate structure 60 is facilitated by the unfired condition of the ceramic cover 48 and substrate 40, which are relatively soft and easily cut in that state. The die cutting operation is thus performed with lower power required

than in conventional methods. In addition, because green ceramic is less brittle than fired ceramic, there is less loss due to cracking and breaking of the ceramic during the cutting operation.

The die cut individual units are then fired as is known in the art to cure the ceramic material. During firing, the heat causes an intermetallic bond to form between the wire elements 50 and the metal film 44, creating a reliable connection.

The individual units 70 are then coated with end terminations to form the fuse 10 of Figs. 1-3. According to a preferred embodiment of the invention, the individual units 70 are positioned by conventional vibratory sorting means in a fixture having a multiplicity of holes for holding the units. The units are held in parallel in the fixture, and the opposite end portions 12, 14 at which the wire elements 50 terminate are dipped and coated with electrical conducting material in one or more steps.

Fig. 9 is a perspective view of a subminiature circuit protector 100, or chip fuse, having multiple substrate layers and fuse elements for higher voltage and/or current capacity.

The fuse 100 includes an upper layer or cover 120, a bottom layer 126 and intermediate layers 122 and 124. The layers 122-126 and cover 120 are

laminated together to form a chip structure. End terminations 30, 32, as previously described, are preferably provided at opposite ends of the fuse 100 electrically connect with the interior components of the fuse 10, not illustrated in this figure.

Although the fuse 100 in Figure 9 is shown with a cover 120 and three lower layers 122, 124 and 126, the number of layers shown is illustrative rather than limiting. As will be understood by the following description, a fuse in accordance with the present invention may include a cover and a plurality of layers.

According to one aspect, each of the layers below the cover 120 carries at least one fusible element. The fusible elements may be connected in series, in parallel, or in a combination series and parallel, as further described below.

Fig. 10a illustrates a first embodiment 112 of the fuse of the invention in which the fusible elements are connected in series. Fig. 10a is a sectional view taken along the line 10-10 of Fig. 9. Fig. 11 is an exploded view of a chip fuse 112 having fusible elements connected in series. The following description refers to both figures.

As may be seen, each layer 122a, 124a and 126a includes a fusible element 140a, 142a and 144a,

respectively. The fusible elements 140a, 142a, 144a are interconnected and are preferably connected to the end terminations 30, 32 by vias 150, 152, 154 and 156 to form a series connection from one end termination 30 to the other end termination 32. The vias 150-156 are holes formed in each layer at predetermined locations and metallized, that is, filled with an electrically conductive metal. As may be seen with attention to Fig. 11, according to one embodiment of the invention, the fusible elements 140a, 142a, 144a are contained within each respective layer 122a, 124a, and 126a, and do not contact the end terminations 30, 32 except through the vias 150 and 156, which are connected to the uppermost 140a and lowermost 144a fusible elements. However, according to another embodiment, if desired or necessary, instead of using the vias 150 and 156 in the embodiment shown in Fig. 10a, the pads 146a may extend directly to the end terminations 30 and 32 as shown by dotted lines in Figs. 10a and 11. The fuse elements may or may not extend to the end terminations as shown in Fig. 10a as desired or necessary. Further still, the end terminations 30, 32 may be wholly omitted and the vias 150 and 156 or pads 146a that extend to ends of the substrate may be

connected directly in the circuit in which the chip fuse is used.

As best seen in Fig. 11, each of the fusible elements 140a, 142a and 144a is formed with spaced apart, enlarged pad portions 146a connected by a narrow strip 148a. The narrow strip 148a, or fuse element, is a thin film of metallic material selected for responsiveness to voltage and/or current. The pad portions 146a comprise a film of metallic material preferably somewhat larger than the fuse element 148a, although the pad portions and the fuse element may be applied in a single print which would result in those elements being the same thickness.

As seen in Fig. 10a, the fuse element 148a is applied beneath, i.e., before the pad portions 146a. However, fuse elements according to the present invention may be applied at the same time as the pad portions, i.e., in a single print, as seen in Fig. 11, or before or after the pad portions, as shown by dotted lines in Fig. 11.

As seen in Fig. 10a and Fig. 11, the chip fuse 112 may have a functional fuse element having an effective length that is the addition of the lengths of the fuse elements 148a of the individual layers 122a, 124a, and 126a. The chip fuse 112 thus is

shorter and more compact than a conventional fuse having the same voltage rating.

Fig. 10b illustrates a second embodiment of a fuse chip 114 having fusible elements connected in parallel, rather than in series as in Fig. 10a. Each of the layers 122b, 124b, and 126b carries a fusible element 140b, 142b, 144b. The fusible elements 140b-144b each include pads 146b at opposite end portions connected by a thin fuse element 148b. The pads 146b extend to the ends of each layer 122b, 124b, 126b, to contact the adjacent end terminations 30, 32 at the opposite ends of the chip fuse 114. The pads 146b may also extend laterally to lateral edges of each layer to contact the portion of the end terminations covering the lateral edges, thus making contact with the end terminations 30, 32 on three sides.

As shown in Fig. 10b, each of the fusible elements 140b, 142b, 144b of each layer is connected with both of the end terminations 30, 32. The chip fuse 114 therefore has a plurality of parallel connected fuse elements. The fuse chip 114 of Fig. 10b may thus be configured for higher current carrying capacity because of the multiple parallel current pathways.

In each of the chip fuses 112 and 114, the end terminations 30, 32 are preferably formed of three

layers of electrically conductive material as described in connection with the single layer fuse 10, above. Also, the end terminations 30, 32 may be wholly omitted and the chip fuses may be connected to a circuit directly to the vias 150, 156 or pads 146a or 146b extending to the ends of the substrates. Further, if desired or necessary, the chip fuses may be provided with, for example, a coating of silver or a silver alloy proximate the ends of the chip fuses such that the coating contacts the vias or the pads, and the chip fuses may be inserted in a socket or a clip for connection to an electrical circuit.

Fig. 12 is a top view of a substrate layer 160 for a chip fuse according to an alternative embodiment of the invention. The fusible element is formed thereon as two fuse elements 162, 164 connected in series. Pads 146c at the opposite ends of the substrate 160 extend to the end edges and both lateral edges of the substrate layer. A third pad 166 is disposed on the substrate 160 substantially centrally. The two fuse elements 162, 164 connect to the end pads 146c and center pad 166 to form the two fusible elements in series. A plurality of substrate layers 160 may be laminated in a single chip fuse in the manner illustrated in Fig. 10b, that is, for parallel connection of the fuse elements of each

layer. A chip fuse having substrate layers 160 thus has a combination of series and parallel connections.

Fig. 13 is a top view of another alternative embodiment of a substrate layer 170. Pads of electrically conductive film are disposed on the opposite end portions of the substrate 170. Two fusible elements 172 and 174 are deposited on the upper surface of the substrate 170 in parallel and connect to both of the pads 146d. The substrate layers 170 are formed with metallized holes in predetermined locations as described in connection with Fig. 10a. A plurality of substrate layers 170 may be assembled in the manner described in connection with Fig. 10a to form a chip having a combination parallel and series fuse connections.

Figs. 14 and 15 illustrate a method of manufacturing multiple layer fuses 112, 114. Fig. 14 relates to the chip fuse 112 described in connection with Fig. 10a, and Fig. 15 relates to the chip fuse 114 described in connection with Fig. 10b. The method permits the manufacture of a multiplicity of individual fuses starting with a plurality of substrate layers.

Referring to Fig. 14, a substrate layer 180 of green, or unfired, ceramic material having an upper surface 182 is provided. A multiplicity of pads 184

and fuse elements 186 are deposited on the upper surface 182 in spaced relationship. The fuse elements 186 connect two adjacent pads to form a fusible element for the individual substrate layers, as previously described. The pads and fuse elements may be deposited in individual steps or simultaneously in a single step by screen printing or another suitable method. The substrate layer 180 may also be printed with a multiplicity of fuse elements 172, 174, and pads 146d, illustrated in Fig. 13.

A plurality of substrate layers 180 are prepared to provide, for example, layers 122a, 124a, 126a as shown in Fig. 10a and Fig. 11. The individual layers are punched to place holes for the metallized vias 150-156 to interconnect the fuse elements of the layers. As may be understood by reference to Fig. 11, different patterns of holes are punched in a substrate layer depending on which the position the layer will take in the formed chip fuse to facilitate the interconnecting of the fuse elements.

The holes may be metallized by drawing a paste of electrically conductive metal through the holes by vacuum, or by another suitable method. The holes are preferably punched and metallized before the pads and fuse elements are deposited on the substrate layer, although the pads and fuse elements may be put on

prior to forming holes and metallizing the holes or prior to metallizing formed holes.

A plurality of substrate layers 180 is assembled in a stack, and positioned so the pads 184 and fuse elements 186 are positioned in overlaying relationship as suggested by the single chip fuse in Fig. 11. A cover layer of green ceramic is applied to a top one of the substrate layers. The cover layer of green ceramic may be applied before or after the assembled substrate layers are bonded together. The assembled structure is then cut or diced into individual units, in the manner indicated by the broken lines in Fig. 14, so that each unit contains a plurality of fuse elements in a stack.

A steel rule die, or other suitable tool, is preferably used to cut the laminate structure into individual units as described above for the single layer fuse 10.

The individual units are then fired as was described above to cure the ceramic material. During firing, the heat causes a metallic bond to form between the vias 150-156 and the metal film pads 146a, creating a reliable electrical connection.

The individual units are then coated with end terminations to form the fuse 100 shown in Fig. 9 and Fig. 10a, in accordance with the description above.

Referring to Fig. 15, a method of making a fuse chip according to Fig. 10b is described. A substrate layer 190 of green, or unfired, ceramic material having an upper surface 192 is provided. Electrically conductive metal film is deposited on the upper surface 192 as a plurality of spaced, preferably parallel columns 194 to provide what will form the end pads 146b in the completed chip fuse illustrated in Fig. 10b.

Additional conductive metal film is deposited on the upper surface 192 in a plurality of spaced, preferably parallel rows 196, the rows being oriented perpendicular to the columns 194. The rows 196 form, for example, what are the fuse elements 140b, 142b, 144b, in the completed chip fuse shown in Fig. 10b. The substrate layer 190 may also be printed with the fuse elements 162, 164, and central pad 166 illustrated in Fig. 12.

A plurality of substrate layers 190 may be assembled in a stack with the columns and rows in the layers being aligned. A cover of green ceramic is applied on an uppermost substrate layer to form an assembled structure. The substrate layers 190 may be pressed together to bond to one another before or after the cover of green ceramic is applied. The substrate layers 190 and the cover 120b of green

ceramic are preferably bonded together under heat and pressure. The assembled structure is cut or diced as described above, in a pattern as indicated by the broken lines in Fig. 15 to form individual units.

The individual units are fired to cure the ceramic, and the fired units are coated with the end terminations as described above.

The present invention is not limited to embodiments wherein a fuse element is disposed on each substrate layer. As seen in Fig. 16, which shows a chip fuse 212 having fuse elements 240a, 242a and 244a connected in series, although the fuse elements may, instead be connected in parallel, a fuse element may be omitted on one or more layers 222a, 224a, 226a, 228a, which might be desired, for example, to minimize the possibility of arcing between fuse elements. Moreover, if desired or necessary, a fuse element may be printed on both sides of a single layer 222a, 224a, 226a, or 228a which may be desired, for example, to increase the working length of series connected fuse elements, or on a top side of one substrate layer and a bottom side of another layer within the same chip fuse.

The foregoing has described the preferred principles, embodiments and modes of operation of the present invention; however, the invention should not

be construed as limited to the particular embodiments discussed. Instead, the above-described embodiments should be regarded as illustrative rather than restrictive, and it should be appreciated that variations, changes and equivalents may be made by others without departing from the scope of the present invention as defined by the following claims.

WHAT IS CLAIMED IS:

1. A method for making chip fuses, comprising the steps of:

forming at least one substrate element of green ceramic material;

disposing on the upper surface of at least one substrate element a plurality of spaced columns of electrically conductive film and a plurality of rows of electrically conductive elements in a spaced relationship to one another and in a direction substantially transverse to a direction of the film columns;

applying a cover of green ceramic material to an upper surface of the substrate to form a laminate structure;

dividing the laminate structure to form a multiplicity of individual chip fuses, each chip fuse including a fuse element comprising pads of metal film at opposed end portions formed from the electrically conductive film and an electrically conductive element connecting the pads formed from the electrically conductive elements; and

firing the chip fuses to cure the green ceramic and to create a metallic bond between the

electrically conductive elements and the conductive metal film pads.

2. The method according to claim 1, wherein the step of disposing the columns and rows on each substrate element is by the steps of:

printing a plurality of spaced columns of electrically conductive film on an upper surface of a green ceramic substrate; and

printing a plurality of electrically conductive elements on the upper surface of the substrate in a spaced relationship to each other and in a direction substantially transverse to a direction of the film columns.

3. The method according to claim 1, wherein the step of disposing columns of film comprises printing columns of separate pads of electrically conductive film; and

the electrically conductive elements are deposited to interconnect two pads.

4. The method according to claim 1, wherein at least two substrate layers are prepared with columns of electrically conductive film and rows of electrically conductive elements, said substrate

layers are positioned in layers to form a laminate structure so that said electrically conductive elements of each layer are in alignment; and

aligned columns between layers are interconnected at selected locations for electrical conduction therebetween.

5. The method according to claim 4, wherein the step of interconnecting aligned columns between layers, comprises:

forming holes in each substrate at predetermined locations of the substrate corresponding to film column locations; and

metallizing said holes, wherein the metallized holes electrically connect columns at predetermined locations in the stacked layers.

6. The method according to claim 5, wherein interconnecting the aligned columns of the layers connects the fuse elements in series in each chip fuse.

7. The method according to claim 6, further comprising the steps of:

providing an end termination to opposite end portions of the fuses after the firing step; and,

electrically connecting a pad at one end of said fuse element series to one of said end terminations, and electrically connecting a pad at an opposite end of said fuse element series to an opposite end termination.

8. The method according to claim 7, wherein the step of connecting said pads to the end terminations comprises providing for each pad a conductor in a hole from said pad through interposed substrates to said termination.

9. The method according to claim 8, wherein the step of providing an end termination comprises:

applying an innermost layer of a silver alloy, a layer of nickel over the innermost layer, and a layer of a tin/lead containing alloy over the nickel layer.

10. The method according to claim 1, further comprising the step of providing an end termination to opposite end portions of the fuses after the firing step, wherein the end termination is in electrical contact with at least one pad of the metal film at each opposite end portion.

11. The method according to claim 10, wherein the step of providing an end termination comprises:

applying an innermost layer of a silver alloy, a layer of nickel over the innermost layer, and a layer of a tin/lead containing alloy over the nickel layer.

12. The method according to claim 1, further comprising the step of applying to each end portion a coating having an innermost layer of a silver alloy, a layer of nickel over the innermost layer, and a layer of a tin/lead containing alloy over the nickel layer to form end terminations.

13. The method according to claim 1, wherein

the step of dividing the laminate structure is performed so that each chip fuse includes opposite end faces and opposite lateral faces and each pad of metal film on each layer extends to one end face and both lateral faces, and

the step of providing the end termination connects the pads of each layer at opposing end portions so that the fuse elements of each fuse chip are connected in parallel.

14. The method according to claim 1, wherein the step of disposing a plurality of fuse elements

comprises rolling a plurality of wire fuse elements on the substrate.

15. A chip fuse, comprising:

a plurality of substrate layers of ceramic material each having an upper surface, said substrate layers being arranged in a stack having at least an uppermost and lowermost substrate layer;

a fuse element of electrically conductive material disposed on the upper surface of two or more of said substrate layers;

a cover of ceramic material covering an upper surface of the uppermost substrate layer, wherein said substrate layers and cover form a laminate structure having first and second end portions; and

means for electrically interconnecting said fuse elements of the plurality of substrate layers.

16. The chip fuse as claimed in claim 15, further comprising:

end terminations of electrically conducting material proximate said first and second end portions of the laminate structure;

means for electrically connecting at least an uppermost fuse element to a first of said end terminations; and

means for electrically connecting at least a lowermost fuse element to a second of said end terminations.

17. The chip fuse as claimed in claim 16, wherein on each substrate layer said fuse element extends from a first edge at said first end portion to an opposite second edge at said second end portion of the substrate; and,

said end terminations at said first and second end portions electrically connect with said fuse elements on each of said substrate layers, wherein said fuse elements are interconnected by the end terminations.

18. The chip fuse as claimed in claim 17, wherein

said fuse elements each comprise a pad of electrically conductive material disposed at each of the first and second end portions of said substrate, said pads extending to at least said first and second edges, and a fusible element disposed between and electrically connecting said pads.

19. The chip fuse as claimed in claim 18, wherein said pads on said substrates each further

extend to lateral edges of the first and second end portions.

20. The chip fuse as claimed in claim 17, wherein

said fuse elements each comprise a pad of electrically conductive material disposed at each of first and second end portions of the substrate layer, said pads extending to at least said first and second edges, a third pad of electrically conductive material positioned between and separate from the pads at the first and second end portions, a first fusible element disposed between and electrically connecting the pad at said first end portion with said third pad, and a second fusible element disposed between and electrically connecting the pad at said second end portion with said third pad.

21. The chip fuse as claimed in claim 15, wherein

each of said fuse elements comprises a pad of electrically conductive material disposed at each of a first and a second end portion of said first substrate, and at least one fusible element electrically connecting said pads.

22. The fuse chip as claimed in claim 21, wherein said means for electrically interconnecting the fuse elements comprises a plurality of conductors each disposed in one of a plurality of holes extending through the substrate layers in predetermined locations to electrically connect the fuse elements of adjacent substrate layers.

23. The chip fuse as claimed in claim 15, wherein

each of said fuse elements comprises a pad of electrically conductive material disposed at each of a first and a second end portion of said first substrate, and at least one fusible element electrically connecting said pads,

said means for electrically interconnecting the fuse elements comprises a plurality of conductors each disposed in one of a plurality of holes extending through the substrate layers in predetermined locations to electrically connect the fuse elements of adjacent substrate layers,

said means for electrically connecting at least an uppermost fuse element to the end termination at the first end portion comprises a conductor disposed in a hole extending from a pad on the uppermost substrate layer through the uppermost substrate layer

and intervening substrate layers to the end termination; and

said means for electrically connecting said lowermost fuse element to the end termination at the second end portion comprises a conductor disposed in a hole extending from a pad on said lowermost substrate layer through the lowermost substrate layer to the end termination at the second portion.

24. The chip fuse as claimed in claim 23, wherein a bottom surface of the first and second end portions of the lowermost substrate includes a layer of electrically conductive metal to facilitate electrical connection between the conductors and the end terminations.

25. The chip fuse as claimed in claim 16, wherein the end terminations each comprise an inner layer of silver/silver alloy, a middle layer of nickel and an outer layer of tin/lead containing material.

26. The chip fuse as claimed in claim 15, wherein an end of at least one fuse element extends to one of the first and second end portions of the laminate structure.

27. The chip fuse as claimed in claim 15, wherein a fuse element is disposed on the upper surface of each of said substrate layers.

28. The chip fuse as claimed in claim 15, wherein each of said substrate layers has a lower surface, a fuse element being disposed on the lower surface of at least one of said substrate layers.

FIG. 1

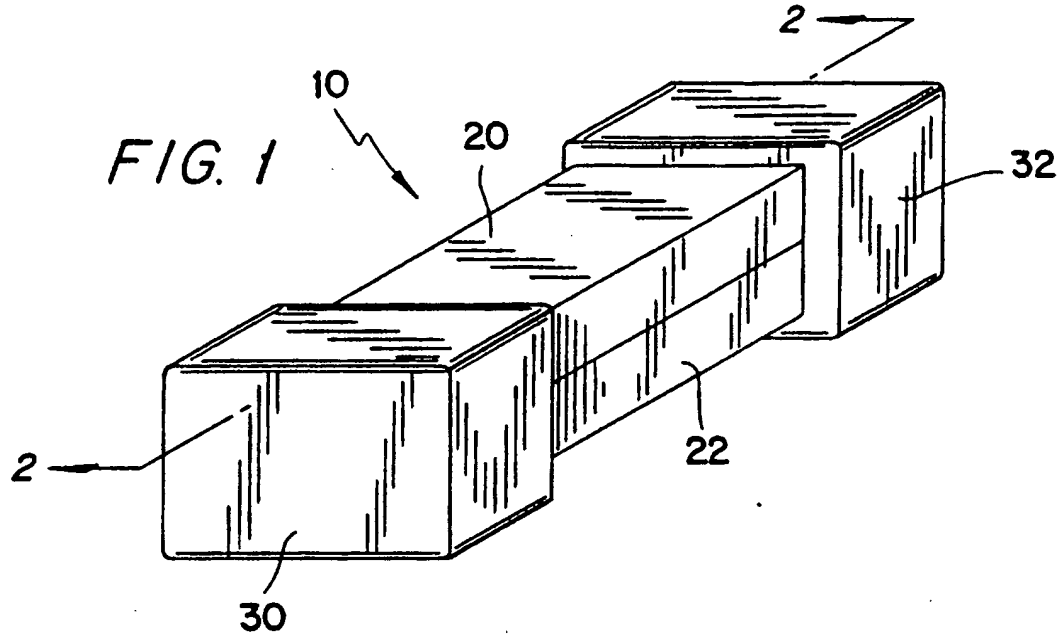
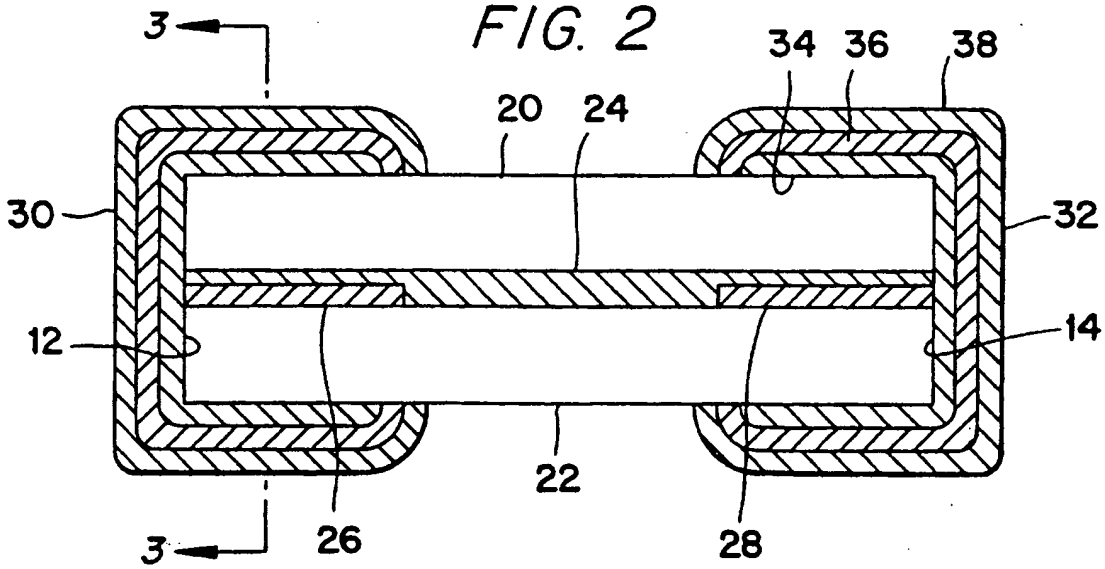


FIG. 2



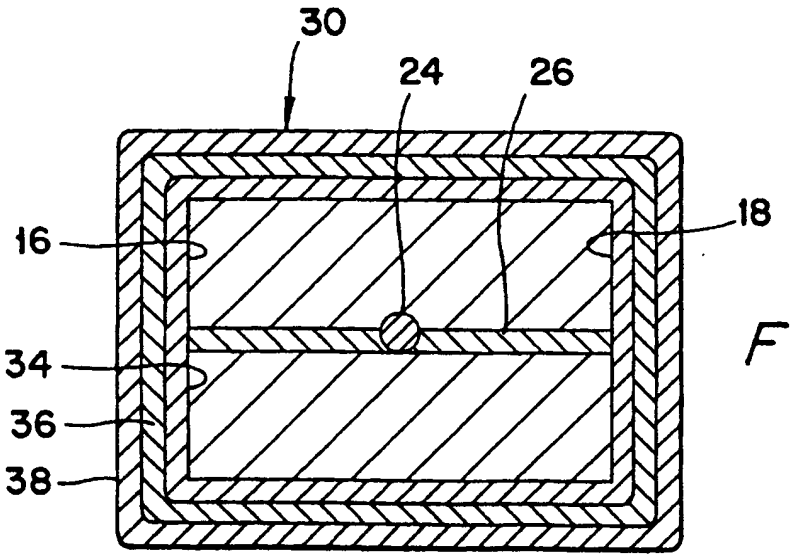


FIG. 3

FIG. 4

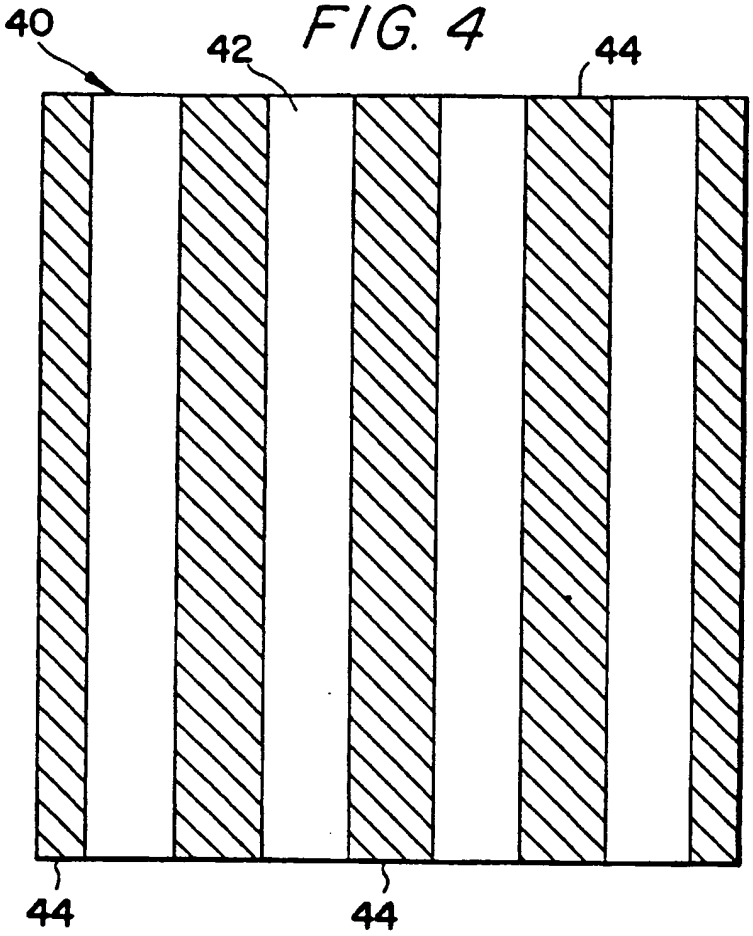


FIG. 5

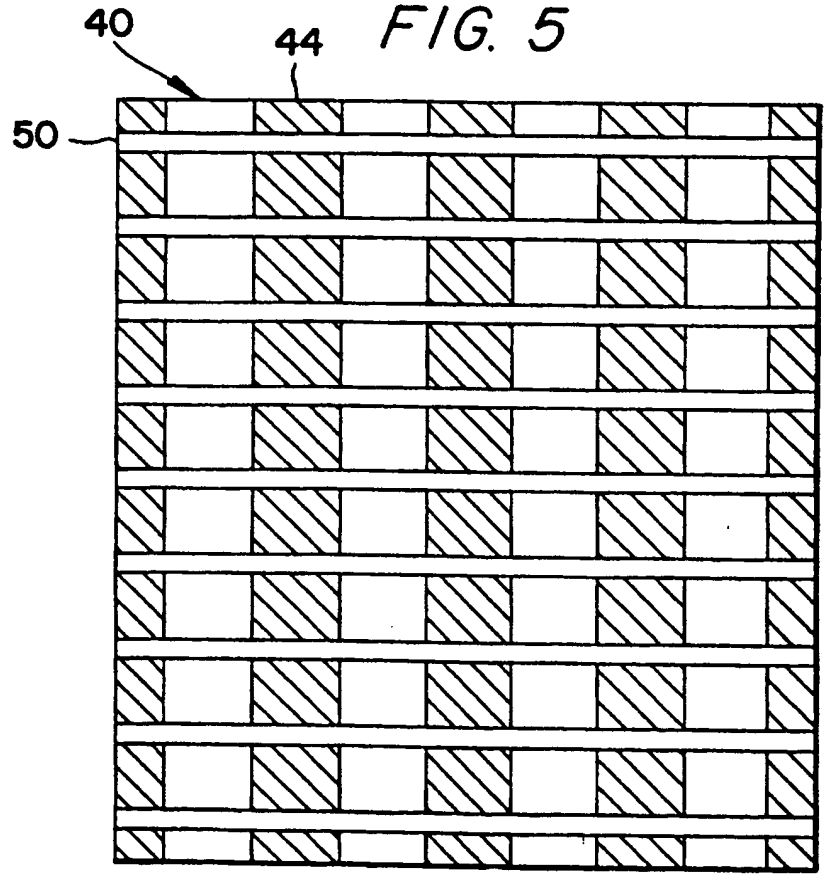


FIG. 6

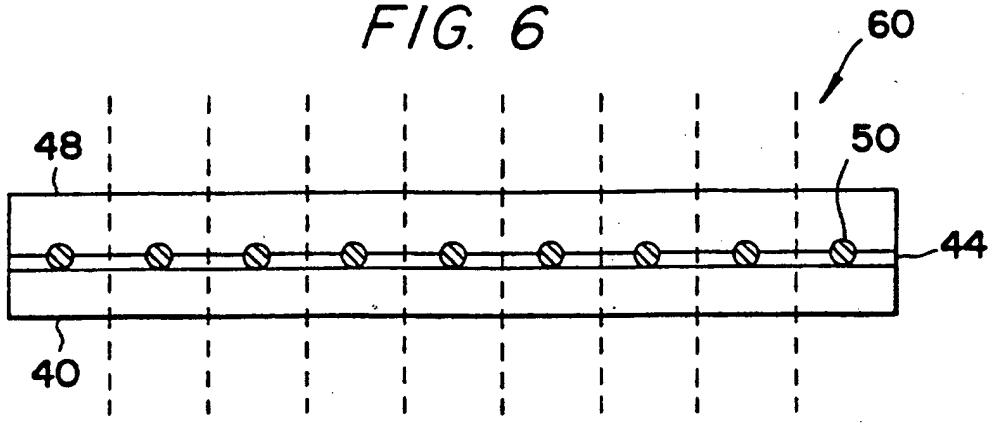


FIG. 7

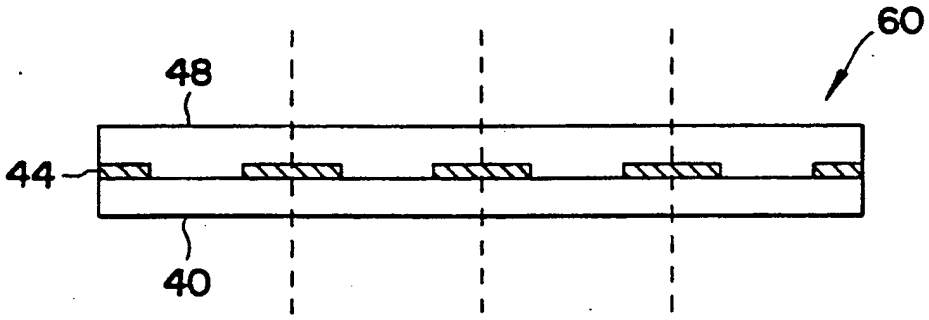


FIG. 8

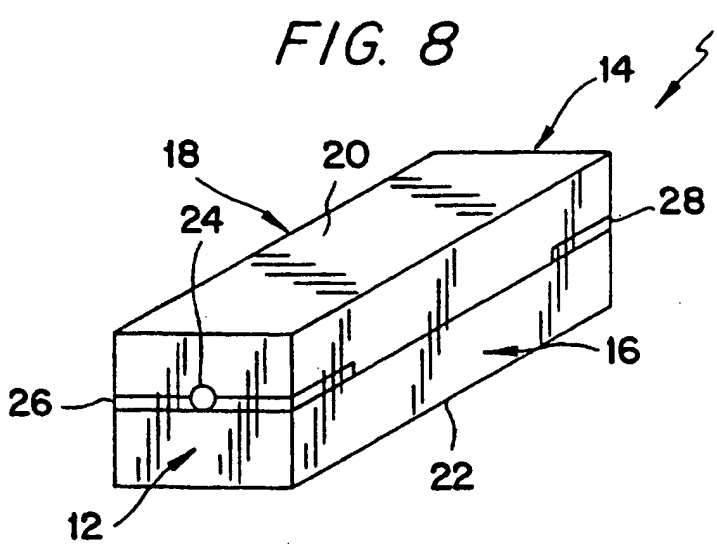


FIG. 9

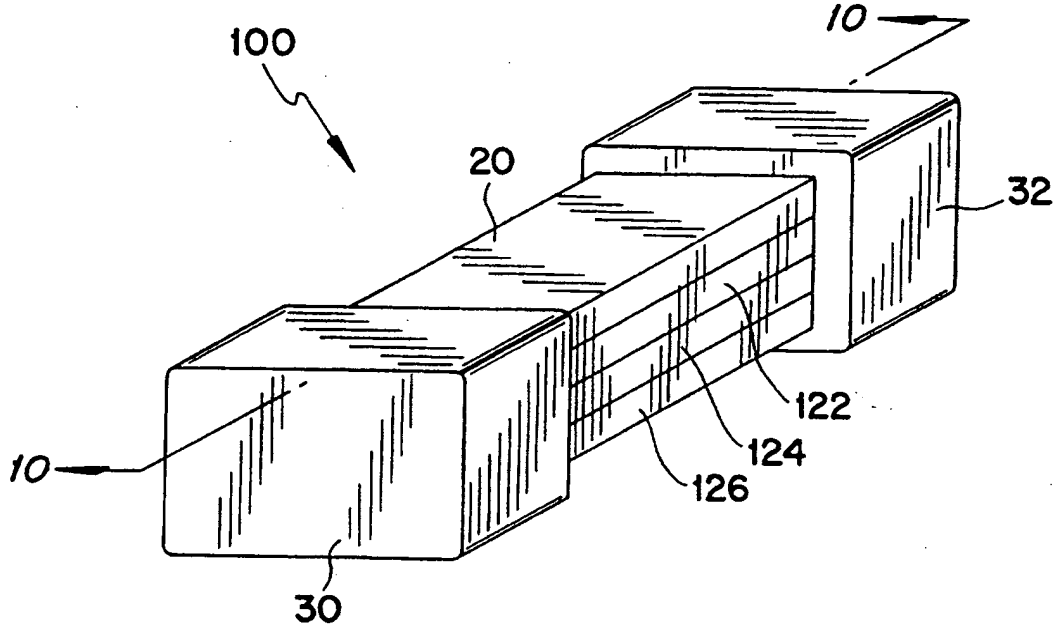


FIG. 10a

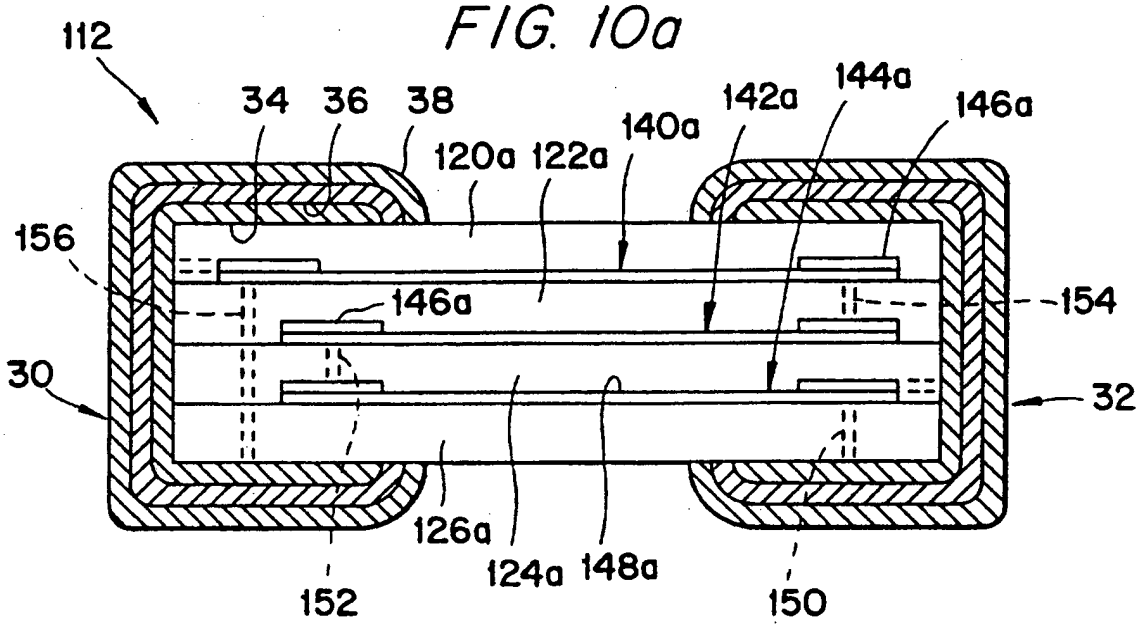


FIG. 10b

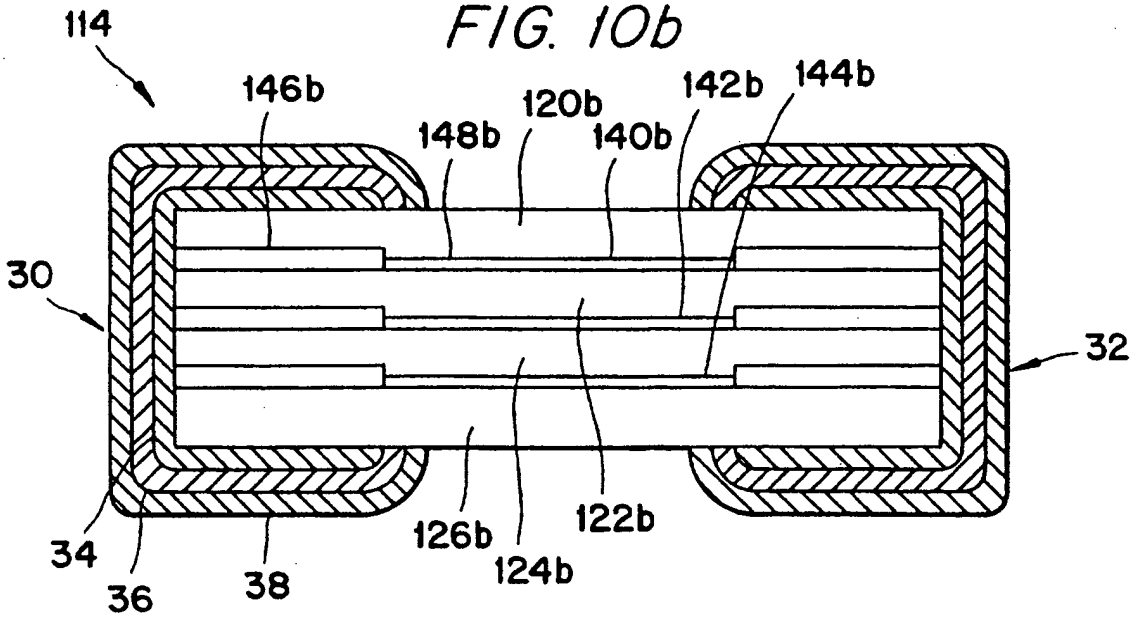
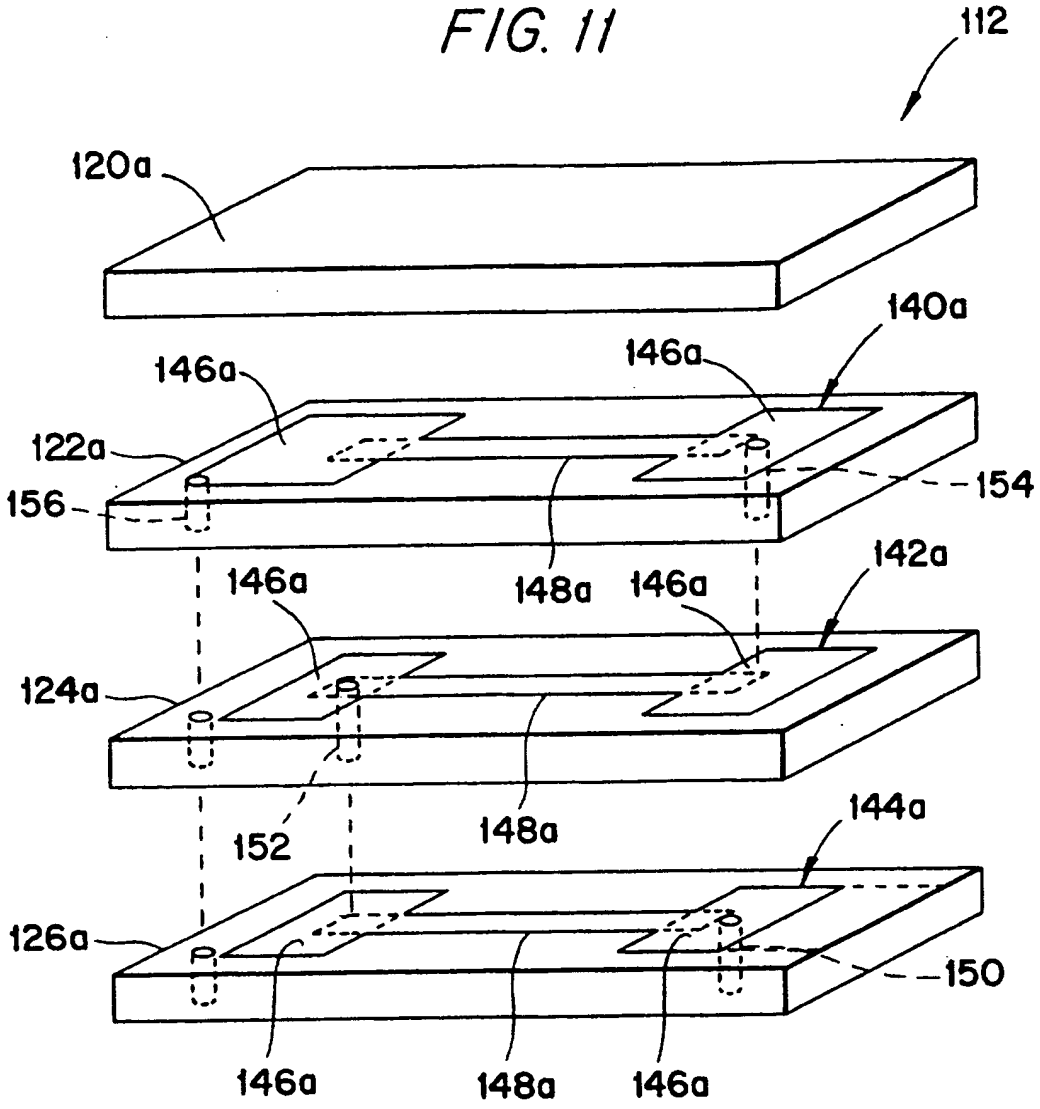


FIG. 11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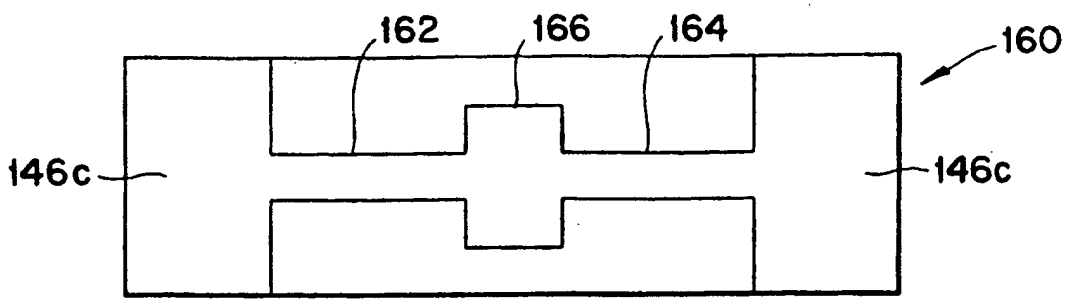


FIG. 12

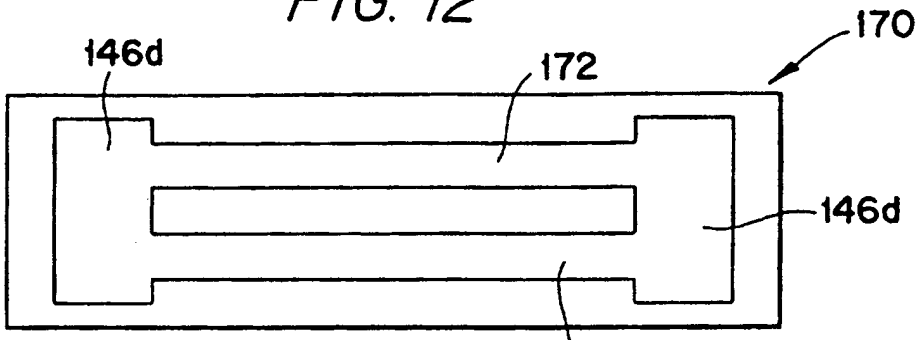


FIG. 13

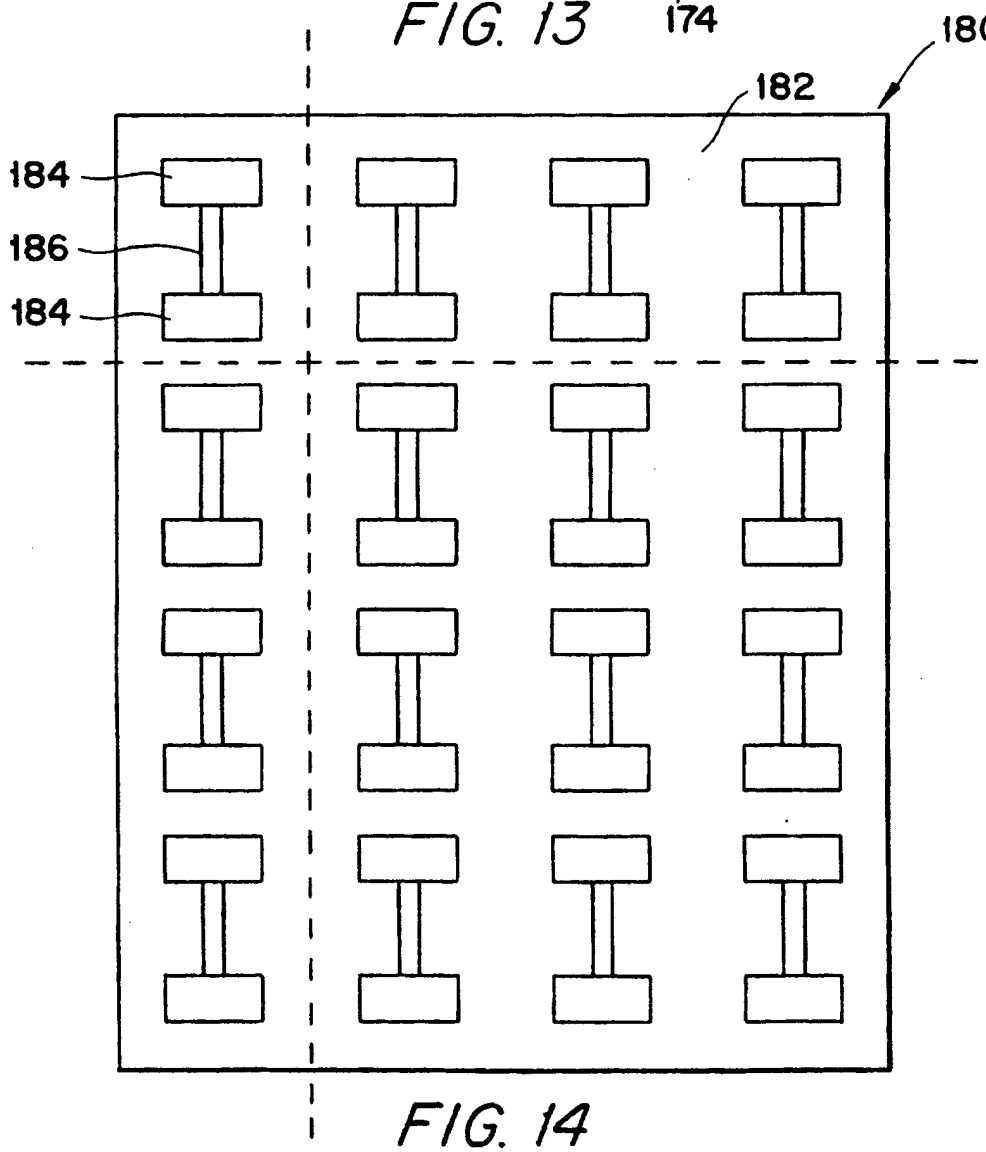


FIG. 14

FIG. 15

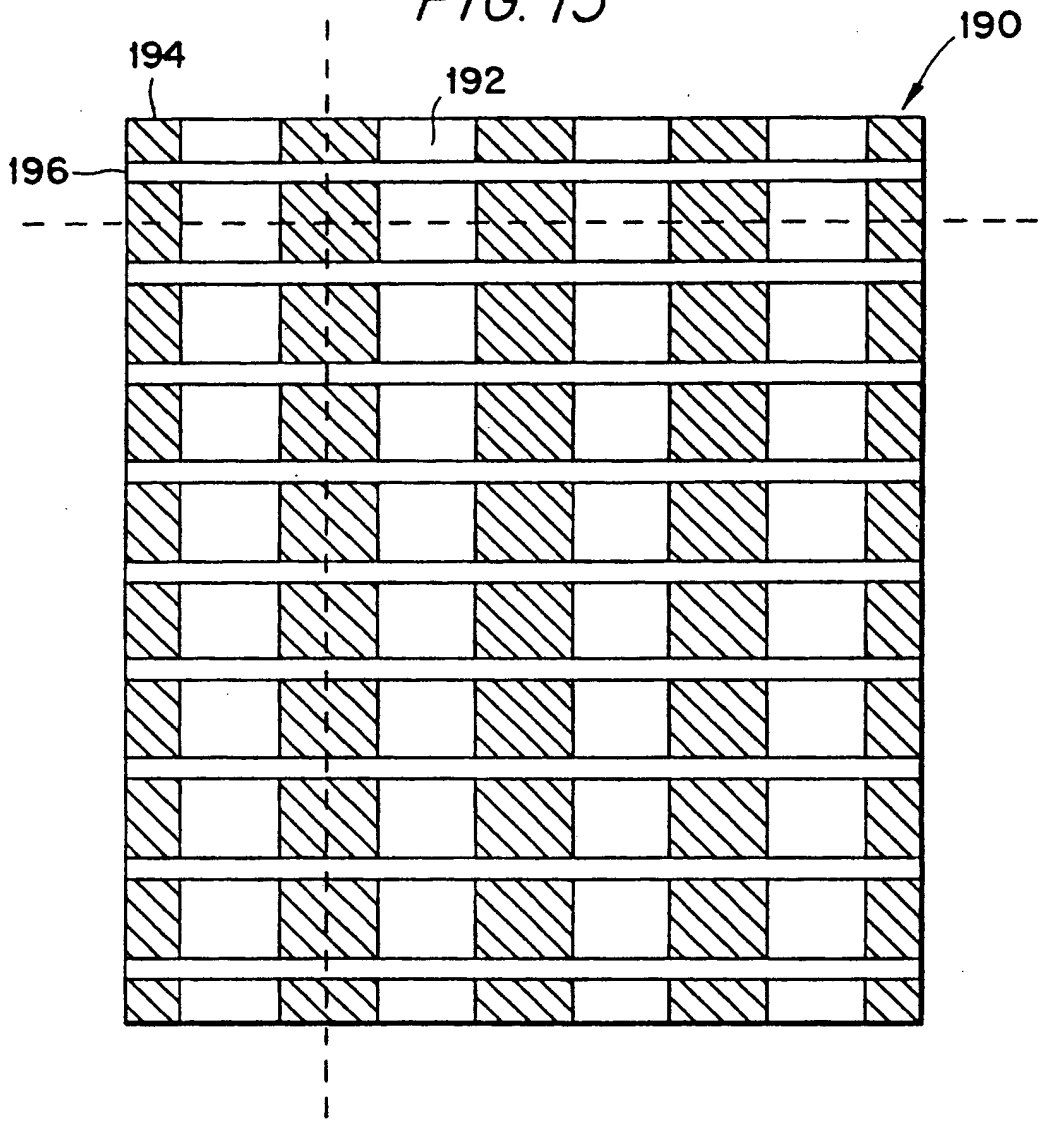
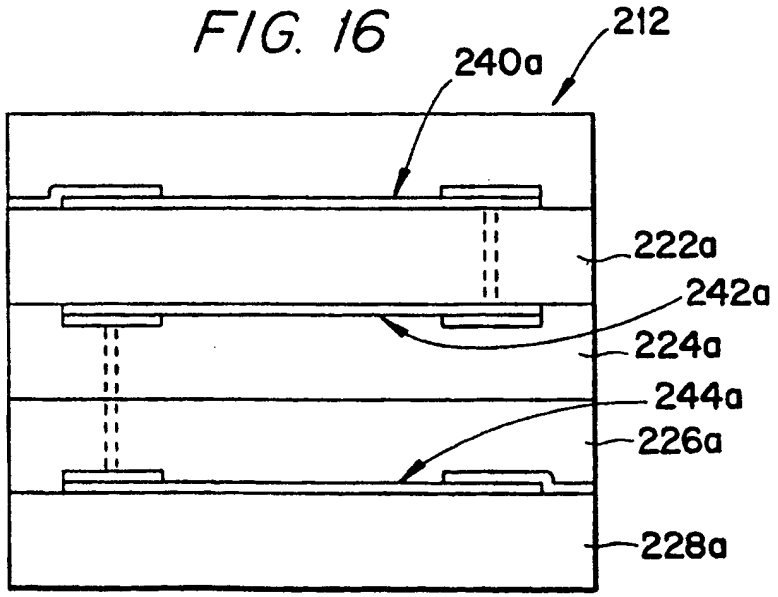


FIG. 16



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/11722

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01H 61/02, 85/04
US CL : 29/623; 337/297
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 29/623, 610.1, 621, 846; 337/227, 296, 297; 264/61

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS
SEARCH TERMS: FUSE?, LAMINAT?

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 3,526,541 (PELTZER) 01 SEPTEMBER 1970	
A	US, A, 5,166,656 (BADIHI ET AL.) 24 NOVEMBER 1992	
A	US, A, 3,777,370 (WAKUI) 11 DECEMBER 1973	
A	US, A, 4,873,506 (GUREVICH) 10 OCTOBER 1989	
A	US, A, 5,228,188 (BADIHI ET AL.) 20 JULY 1993	

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 DECEMBER 1995	11 JAN 1996

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